



# STD22NM20N

## N-CHANNEL 200V - 0.088Ω - 22A DPAK ULTRA LOW GATE CHARGE MDmesh™ II MOSFET

**Table 1: General Features**

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STD22NM20N	200 V	< 0.105 Ω	22 A

- WORLDWIDE LOWEST GATE CHARGE
- TYPICAL R<sub>DS(on)</sub> = 0.088 Ω
- HIGH dv/dt and AVALANCHE CAPABILITIES
- LOW INPUT CAPACITANCE
- LOW GATE RESISTANCE

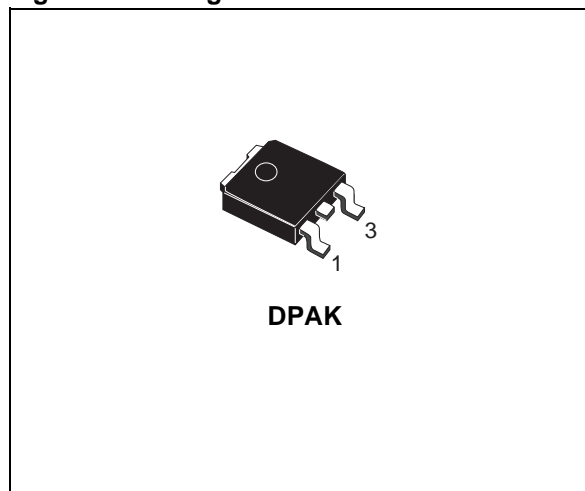
### DESCRIPTION

This 200V MOSFET with a new advanced layout brings all unique advantages of MDmesh technology to lower voltages. The device exhibits worldwide lowest gate charge for any given on-resistance. Its use is therefore ideal as primary switch in isolated DC-DC converters for Telecom and Computer applications. Used in combination with secondary-side low-voltage STripFET™ products, it contributes to reducing losses and boosting efficiency.

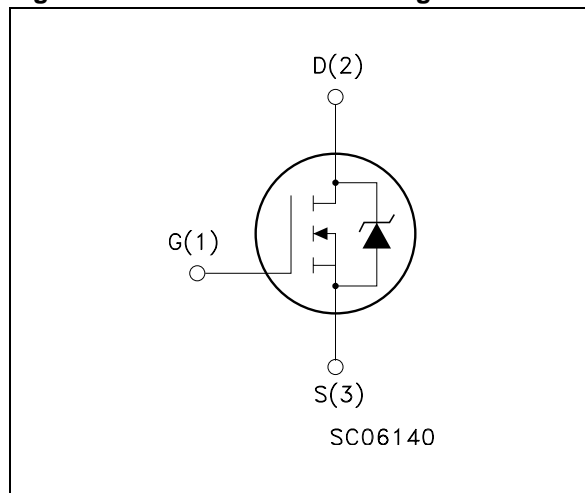
### APPLICATIONS

The MDmesh™ family is very suitable for increasing power density allowing system miniaturization and higher efficiencies

**Figure 1: Package**



**Figure 2: Internal Schematic Diagram**



**Table 2: Order Codes**

SALES TYPE	MARKING	PACKAGE	PACKAGING
STD22NM20NT4	D22NM20N	DPAK	TAPE & REEL

**Table 3: Absolute Maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source Voltage ( $V_{GS} = 0$ )	200	V
$V_{DGR}$	Drain-gate Voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	200	V
$V_{GS}$	Gate- source Voltage	$\pm 20$	V
$I_D$	Drain Current (continuous) at $T_C = 25^\circ$	22	A
	Drain Current (continuous) at $T_C = 100^\circ$	13.7	A
$I_{DM} (*)$	Drain Current (pulsed)	88	A
$P_{TOT}$	Total Dissipation at $T_C = 25^\circ\text{C}$	100	W
	Derating Factor	0.8	W/ $^\circ\text{C}$
$dv/dt (2)$	Peak Diode Recovery voltage slope	14	V/ns
$T_j$ $T_{stg}$	Storage Temperature	150	$^\circ\text{C}$
	Max Operating Junction Temperature	-65 to 150	$^\circ\text{C}$

(\*)  $I_{SD} \leq 22\text{A}$ ,  $di/dt \leq 400\text{A}/\mu\text{s}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$

**Table 4: Thermal Data**

$R_{thj-case}$	Thermal Resistance Junction-case Max	1.25	$^\circ\text{C}/\text{W}$
$R_{thj-amb}$	Thermal Resistance Junction-ambient Max	100	$^\circ\text{C}/\text{W}$
$R_{thj-ambT_l}$	Thermal Resistance Junction-pcb (*)	43	$^\circ\text{C}/\text{W}$
	Maximum Lead Temperature For Soldering Purpose	275	$^\circ\text{C}$

(\*) When mounted on 1 inch<sup>2</sup> FR-4 board, 2 oz Cu,  $t \leq 10 \text{ sec}$

**Table 5: Avalanche Characteristics**

Symbol	Parameter	Max Value	Unit
$I_{AS}$	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by $T_j \text{ max}$ )	22	A
$E_{AS}$	Single Pulse Avalanche Energy (starting $T_j = 25^\circ\text{C}$ , $I_D = 22 \text{ A}$ , $V_{DD} = 50 \text{ V}$ )	380	mJ

**ELECTRICAL CHARACTERISTICS** ( $T_{CASE} = 25^{\circ}C$  UNLESS OTHERWISE SPECIFIED)

**Table 6: On/Off**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source Breakdown Voltage	$I_D = 1mA, V_{GS} = 0$	200			V
$I_{DSS}$	Zero Gate Voltage Drain Current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max Rating}$ $V_{DS} = \text{Max Rating}, T_C = 125^{\circ}C$			1 10	$\mu A$ $\mu A$
$I_{GSS}$	Gate-body Leakage Current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20V$			100	nA
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	3.5	4.2	5	V
$R_{DS(on)}$	Static Drain-source On Resistance	$V_{GS} = 10V, I_D = 11 A$		0.088	0.105	$\Omega$

**Table 7: Dynamic**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$g_{fs} (2)$	Forward Transconductance	$V_{DS} = 15 V, I_D = 11 A$		8		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input Capacitance Output Capacitance Reverse Transfer Capacitance	$V_{DS} = 25V, f = 1 \text{ MHz}, V_{GS} = 0$		800 330 130		pF pF pF
$C_{oss \text{ eq.}} (**)$	Equivalent Output Capacitance	$V_{GS} = 0 V, V_{DS} = 0 V \text{ to } 400 V$		225		pF
$R_G$	Gate Input Resistance	$f = 1\text{MHz}$ Gate DC Bias = 0 Test Signal Level = 20 mV Open Drain		5		$\Omega$
$t_{d(on)}$ $t_r$ $t_{r(Voff)}$ $t_f$	Turn-on Delay Time Rise Time Turn-off Delay Time Fall Time	$V_{DD} = 100 V, I_D = 11 A$ $R_G = 4.7\Omega, V_{GS} = 10 V$ (see Figure 15)		40 15 40 11		ns ns ns ns
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD} = 100 V, I_D = 20 A,$ $V_{GS} = 10 V$ (see Figure 19)		32 6 25	50	nC nC nC

(\*\*)  $C_{oss \text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 8: Source Drain Diode**

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM} (1)$	Source-drain Current Source-drain Current (pulsed)				22 88	A A
$V_{SD} (2)$	Forward On Voltage	$I_{SD} = 20 A, V_{GS} = 0$			1.3	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 20 A, di/dt = 100 A/\mu s$ $V_{DD} = 100V, T_j = 25^{\circ}C$ (see test circuit, Figure 17)		160 960 12.8		ns $\mu C$ A
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD} = 20 A, di/dt = 100 A/\mu s$ $V_{DD} = 100V, T_j = 150^{\circ}C$ (see test circuit, Figure 17)		225 1642 15		ns $\mu C$ A

(1) Pulse width limited by safe operating area.

(2) Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %

Figure 3: Safe Operating Area

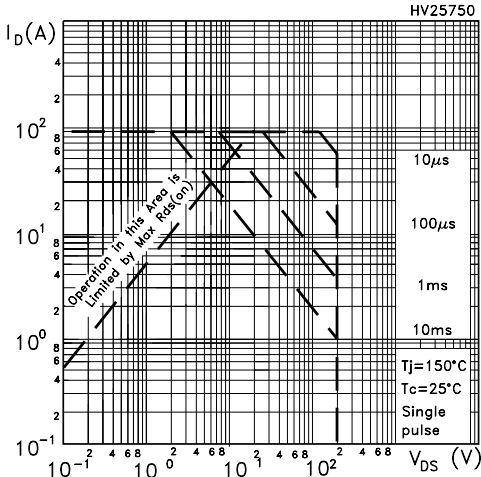


Figure 4: Output Characteristics

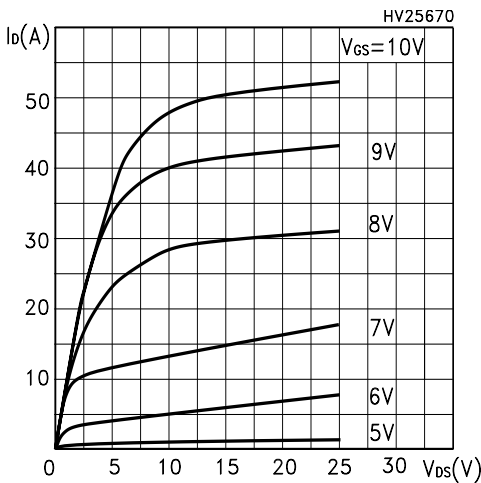


Figure 5: Transconductance

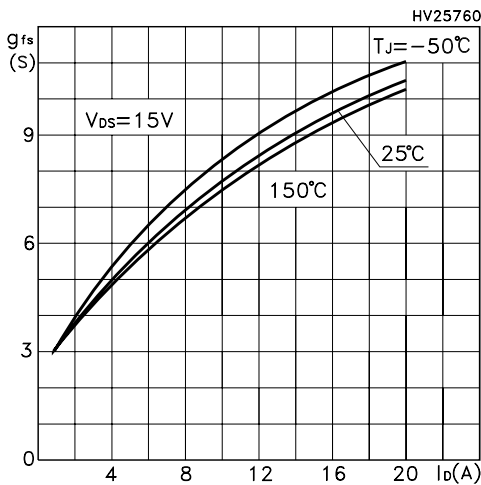


Figure 6: Thermal Impedance

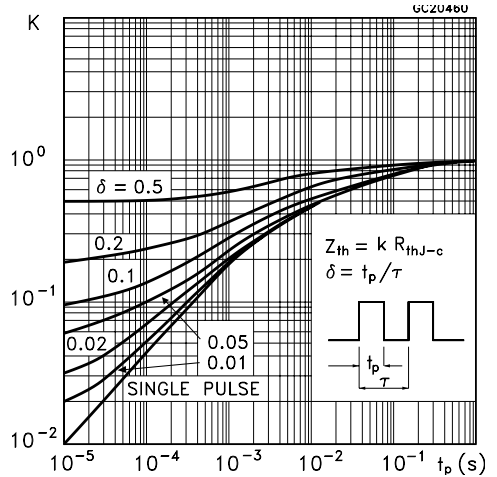


Figure 7: Transfer Characteristics

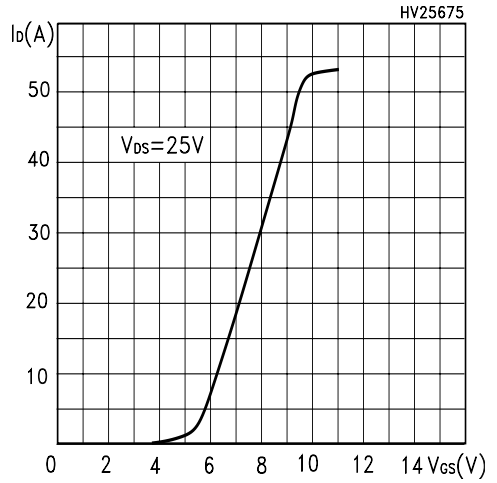


Figure 8: Static Drain-source On Resistance

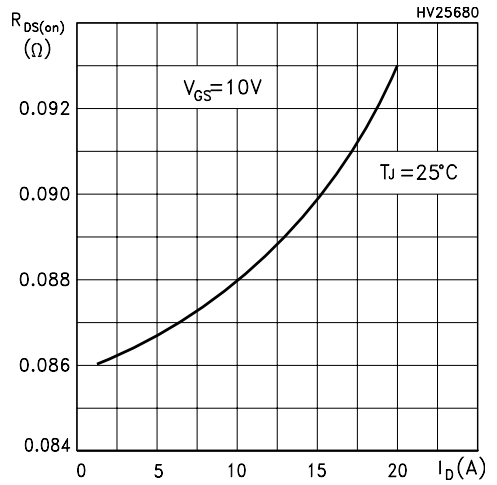


Figure 9: Gate Charge vs Gate-source Voltage

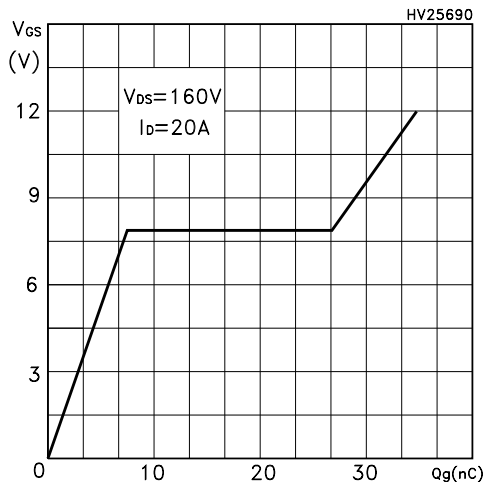


Figure 10: Normalized Gate Threshold Voltage vs Temperature

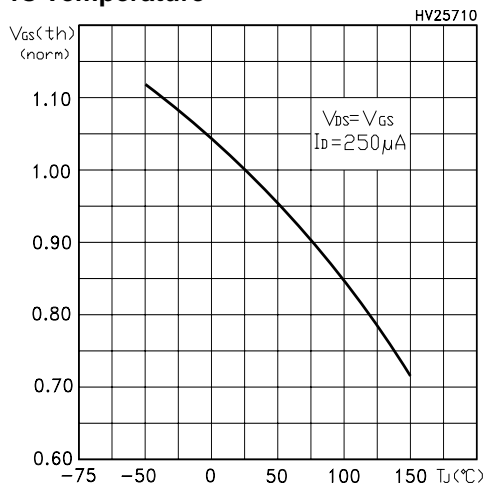


Figure 11: Source-Drain Diode Forward Characteristics

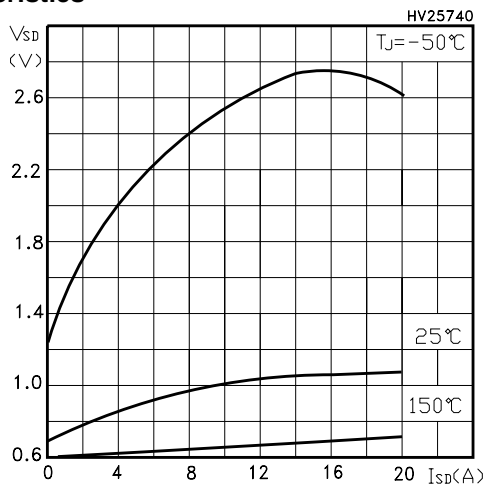


Figure 12: Capacitance Variations

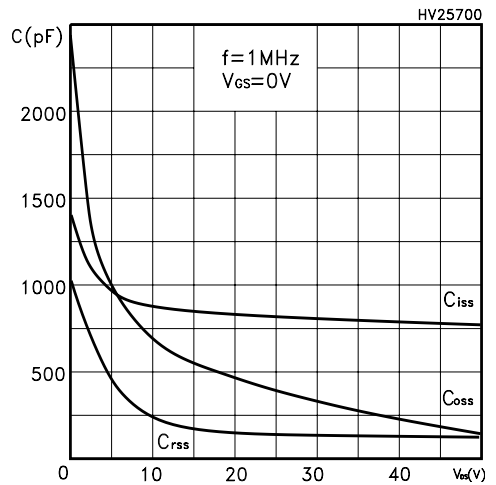


Figure 13: Normalized On Resistance vs Temperature

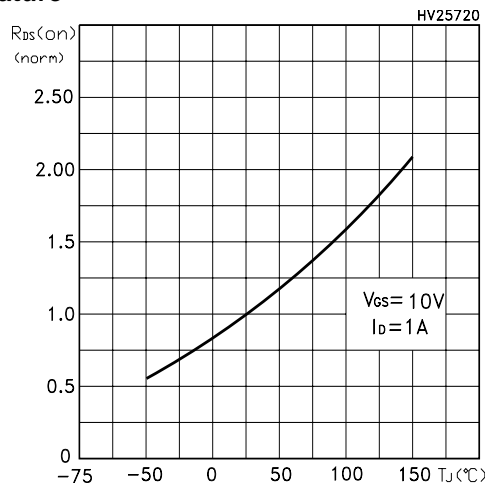


Figure 14: Normalized BVds vs Temperature

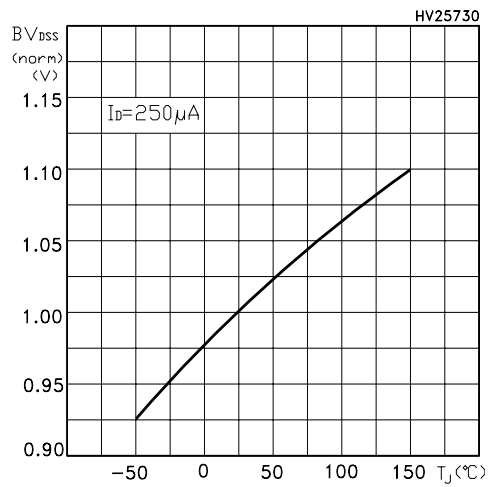


Figure 15: Unclamped Inductive Load Test Circuit

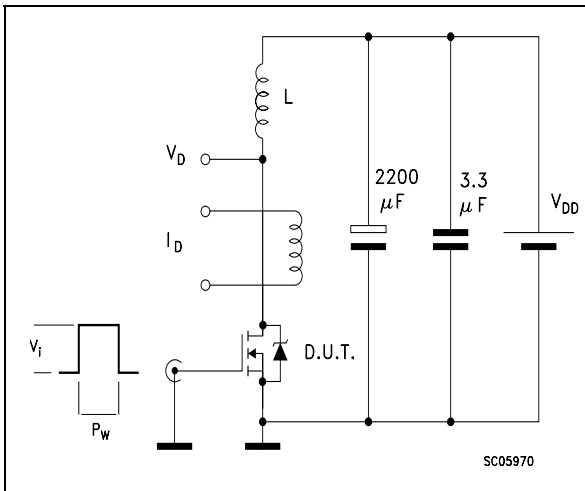


Figure 16: Switching Times Test Circuit For Resistive Load

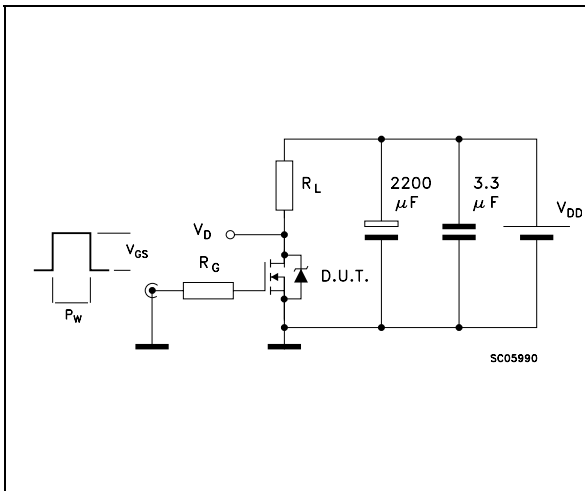


Figure 17: Test Circuit For Inductive Load Switching and Diode Recovery Times

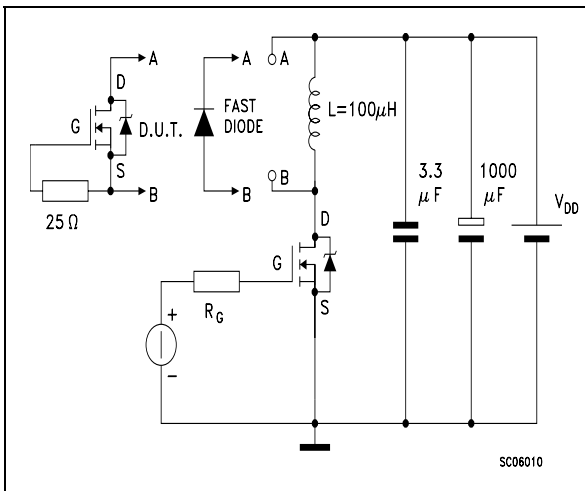


Figure 18: Unclamped Inductive Waferform

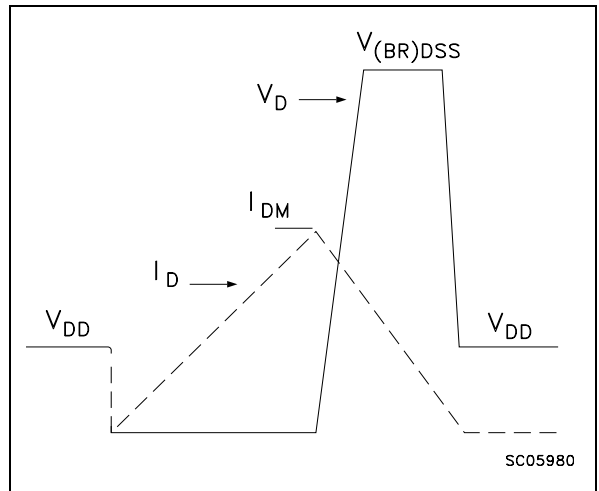
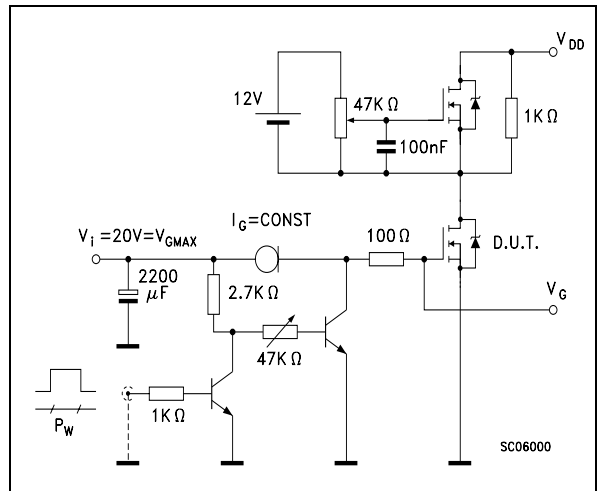
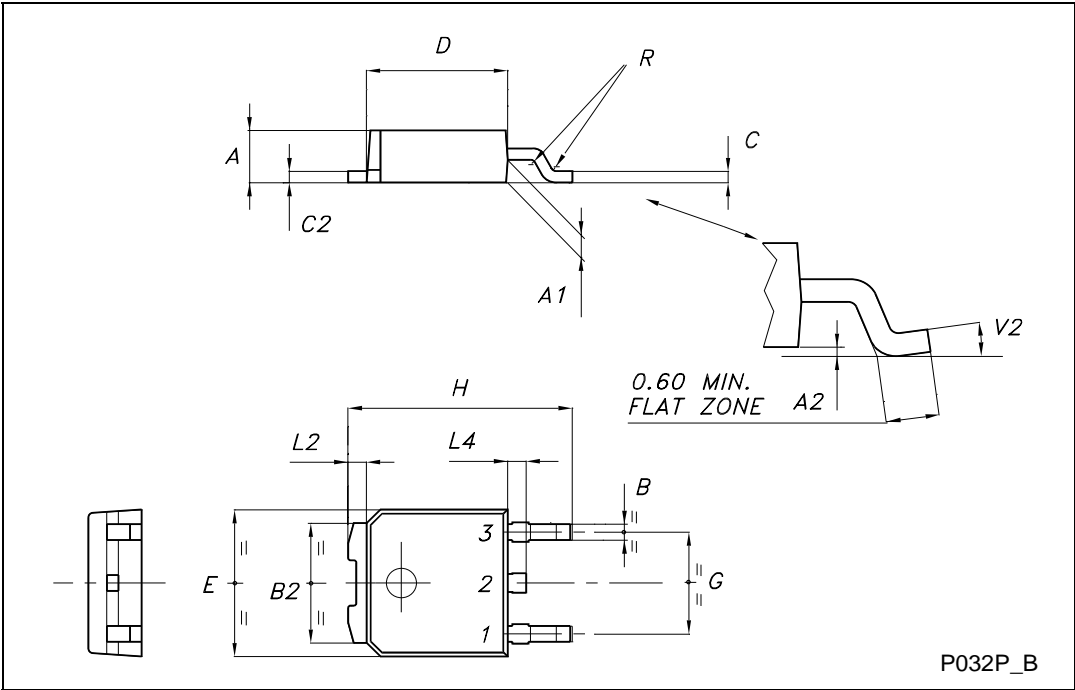


Figure 19: Gate Charge Test Circuit

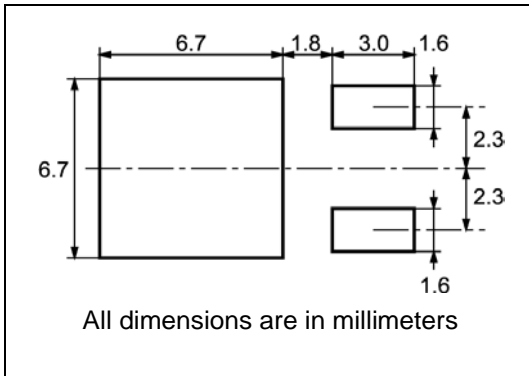


**TO-252 (DPAK) MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
E	6.40		6.60	0.252		0.260
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



**DPAK FOOTPRINT**



**TAPE AND REEL SHIPMENT**

**REEL MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

**TAPE MECHANICAL DATA**

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

**BASE QTY** | **BULK QTY**

2500 | 2500



**Table 9: Revision History**

<b>Date</b>	<b>Revision</b>	<b>Description of Changes</b>
31-May-2004	1	First Release.
15-Mar-2005	2	Update version.
09-May-2005	3	Complete version.
09-Jun-2005	4	New update
04-Nov-2005	5	Corrected value on Table 8

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